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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
NGUYEN, HIEP

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,944	DRAPKIN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8,9,12,13,18-20,22,23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,9,12,13,18-20,22,23 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is responsive to the amendment filed on 06-30-03. Applicant's arguments with respect to references of Bruccoleri (US Pat. 5.808,488) and Diniz et al. (US Pat. 6,107,868) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus the claims remained rejected under Bruccoleri and Diniz.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 6, 8, 9, 12, 13, 18-20, 22, 23 and 25- 27are rejected under 35 U.S.C. 102(b) as being anticipated by Bruccoleri et al. (US Pat. 5,808,488).

Regarding claims 1, 2 and 18, 12 and 22, figure 3 of Bruccoleri shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the step of:

detecting a direction of change of the input voltage at the input of inverter (INV1);

introducing a current to the parasitic capacitance (Cin) when the output of inverter (INV2) becomes high level output when a positive edge of the input signal is applied to the input of inverter (INV1) to charge the parasitic capacitance (Cin) to compensate the current of the input signal charging said parasitic capacitance.

Note that when the input signal voltage rises and is still below the threshold voltage of circuit input, the input parasitic capacitance (Cin) forming by the gate-source/drain of the transistor(s) of inverter (INV1) starts to be charged. When a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of inverter (INV1) becomes low and the output of inverter (INV2) becomes high thus a current is introduced to the parasitic

capacitor (Cin) to compensate for current of the input signal that charges the parasitic capacitor (Cin). The parasitic capacitance (Cin) exists across the input and the ground.

Regarding claims 3,19, 13, 23 and 27, figure 3 of Bruccoleri shows a method of reducing distortion of a signal applied to the input of a circuit having a parasitic capacitance wherein, (INV1) detects a direction of change in voltage of the input signal. Inverter (INV1) has a high output level and inverter (INV2) has low output level in response to a negative edge input signal. The parasitic capacitance (Cin) discharges though inverter (INV2) thus, preventing discharging of the parasitic capacitance into the input signal. The parasitic capacitance (Cin) is considered to exist across the input and the ground.

Regarding claims 5, 6 and 25, figure 3 of Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (INV1) for detecting changes of the input voltage; a correction circuit (INV2) coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance due to the positive edge of the input signal. Note that when the input signal voltage rises and is still below the threshold voltage of circuit input, the input parasitic capacitance (Cin) forming by the gate-source/drain of the transistor(s) of *inverter (INV1) starts to be charged.* When a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of inverter (INV1) becomes low and the output of inverter (INV2) becomes high thus a current is introduced to the parasitic capacitance (Cin) to compensate for current of the input signal that charges (Cin). The parasitic capacitance (Cin) is considered to exist across the input and the ground. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance.

Regarding claims 8, 9 and 20, figure 3 of Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising:

a detection circuit (INV1) for detecting the change of the input signal coupled to the input; and

a correction circuit (INV2) coupled to said detection circuit for compensating for current from the parasitic capacitance (Cin) to be added to the input signal due to a negative edge of the

input signal. Note that when a negative edge of the input is detected, the output of the correction circuit (INV2) goes low thus, the current from the parasitic capacitor (Cin) is discharged through circuit (INV2) and the current from the parasitic capacitance is not added to the input signal. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance. The parasitic capacitor (Cin) appears between said input and ground.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 5, 6, 12, 18, 22, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Diniz et al. (US Pat. 6,107,868).

Regarding claims 1, 2, 18, 12, 22 and 26, figure 3 of Diniz shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the step of:

detecting a direction of change of the input voltage at the input;

introducing a current (64) when a positive edge of the input signal is applied to the gate of transistor (48) to charge the parasitic capacitance, not shown and inherently exists between the gate of and the source of transistor (48), to compensate the current of the input signal charging said parasitic capacitance.

Note that when the input signal voltage rises and is still below the threshold voltage of transistor (48), the parasitic capacitance forming between the gate-source/drain of the transistor (48) is charged. When a rising edge of the input signal is detected to be higher than the input threshold, transistor (48) is turned on and a current (64) is introduced to the parasitic capacitor to compensate for current of the input signal that charges the input parasitic capacitance. The input parasitic capacitance is considered to exist across the input terminal (the gate terminal of transistor 48) and the ground.

Regarding claims 5, 6 and 25, it is inherent that figure 3 of Diniz shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (48) for detecting changes of the input voltage; a correction circuit (44, 46, 49) coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance, not shown, between the gate and the source of transistor (48), due to the positive edge of the input signal. Note that when the input signal voltage rises and is still below the threshold voltage of circuit input, the parasitic capacitance formed between the gate-source/drain of the transistor (48) is charged. When a rising edge of the input signal is detected to be higher than the input threshold, transistor (48) is turned on to activated transistor (46) and current (64) is generated to be introduced to the parasitic capacitance to compensate for current of the input signal that charges it. The parasitic capacitance is considered to exist across the input terminal (the gate of transistor 48) and the ground.

Response to arguments

In the Remarks, the Applicant argues that "Patent '488 teaches a latch specifically designed for use in a comparator" (page 8) and "the '488 Patent does not refer to Cin as a parasitic capacitance but merely as an input capacitance" (page 11). Therefore, the interpretation of Patent '488 is not correct. This statement is not correct for the following reasons:

a. The previous Office Action focuses on the latch comprising cross-coupled inverters (INV1, INV2) that has an effect of introducing a current to the parasitic capacitance (Cin) at the input of the circuit when a positive edge of a signal is applied to the input of inverter (INV1). The basic functioning of a latch having cross-coupled inverter is well known in the art. When a positive edge of a signal is applied to the input of (INV1) of figure 3 of Bruccoleri, the output of inverter (INV2) goes high and a high voltage (Vcc) is applied to the parasitic capacitance (Cin) for compensating the current of the input signal charging the parasitic capacitance (Cin). The circuit of Bruccoleri has the same parasitic capacitance compensation effect as the circuit of figure 2C of the present application does. In figure 2C when a positive edge of an input signal is applied to node (24), transistor (20) is turned on and a high voltage (Vcc) is applied to the

parasitic capacitance (Cp). Through out the Remarks, the Applicant unnecessarily discuses the functioning of the whole circuit of figure 3 of Bruccoleri including the switch system and the output buffers. These elements are not addressed in the 102 (b) rejection. The 102(b) rejection focuses on the latch (INV1, INV2) which is a part of the whole circuit.

b. Capacitor (Cin) is precisely the input parasitic capacitance of the circuit. It is old and well known in the art that the parasitic capacitance is an undesirable by-product of the isolation process during manufacturing of electronic device (see attached reference of Millman and Halkias). The parasitic capacitance exists at the input/output of a device/circuit or any part of a circuit due to conductive wires of the circuit i.e., parasitic capacitances CA and CB of figure 3 of Bruccoleri. In many cases, the parasitic capacitances are not shown in the drawing or they are drawn in dotted lines (Cin) as shown in figure 3.

Because of the above reasons, the rejection under 102(b) using Bruccoleri's reference is proper.

Regarding Patent 6,107, 868 of Diniz et al., again the Applicant argues about the functioning of the whole circuit of figure 3. In the previous Office Action, the Examiner focused only on circuit (92) comprising elements 42, 44, 46, 48 and 49 and the "natural" parasitic capacitance that appears at the gate terminal of transistor 48 (see attached reference of Millman and Halkias). Even though Patent '868 does not point out the parasitic capacitance, the parasitic capacitance at the gate of transistor (48) is well known in the art to exist. Again, for the 102(e) rejection, the Examiner focus only on **circuit (92)** of figure 3. This circuit provides a current to the parasitic capacitance that **inherently** exists at the gate of transistor (48) when a positive edge of an input signal is applied to the input terminal. When a positive edge of the input signal is detected at the gate of transistor (48), transistor (48) is turned on to activate transistor (46), thus current (64) is generated and is introduced to the input parasitic capacitance at the gate of transistor (48).

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M.. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-66251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
09-04-03

TUAN T. LAM
PRIMARY EXAMINER